Optimizing Single-S™ & Total-S™ THD Performance Using Common-mode Capacitors

1. SUMMARY

This application note demonstrates how to increase the Single-Seismic and Total-Seismic (Single-S™ & Total-S™) chipsets exceptional THD performance across possible amplifier gain settings. Optimized performance is achieved by adding simple common-mode filter capacitors on the CS5371/72 and CS5373A Δ-Σ modulator analog inputs. Using a modified Single-S customer demonstration board (CDB5378) to obtain performance data, lab results indicate a THD boost of 2dB (at X4 PGA gain) to 4dB (at X64 PGA gain) is achievable. These results extend to the Total-S chipset because the CS5371/72 and the CS5373A share the same Δ-Σ modulator architecture.

2. MOTIVATION

The need for highly-integrated, low-power, accurate, and reliable seismic data acquisition electronics are fueled by advances in geophysical and seismic signal processing techniques. Cirrus Logic addresses all of these requirements with its Single-S & Total-S chipsets. These chipsets are targeted for data acquisition with signal bandwidths ranging from DC to 2 kHz.

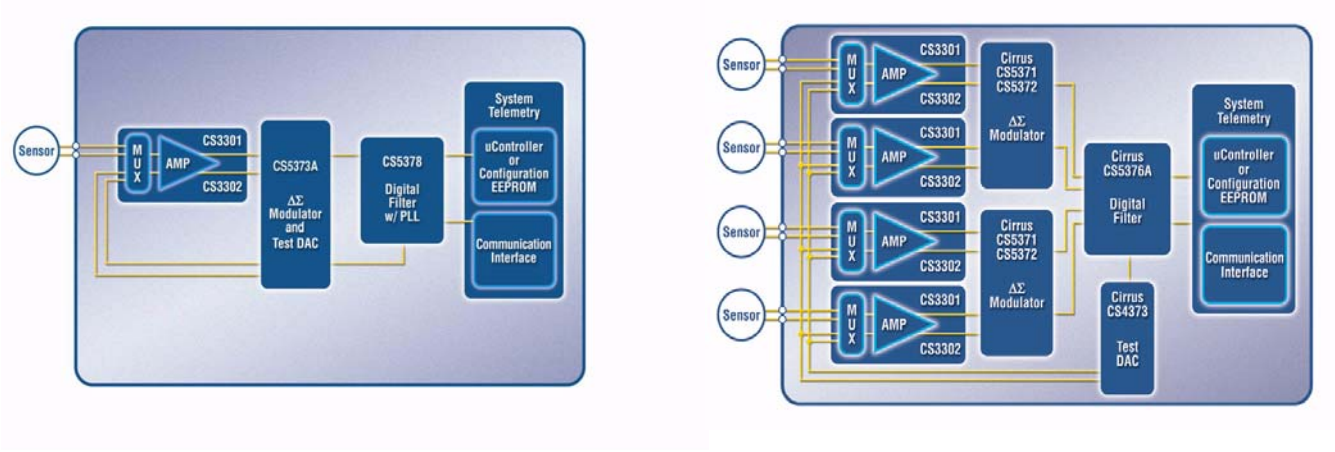

Figure 1. Single-S & Total-S Block Diagrams

Geophysical system designers favor these chipsets because of their power-efficient, high-linearity, and wide-dynamic-range performance. Industry-leading performance can be quantified using the following Single-S customer demonstration board (CDB5378) metric as the benchmark:

- **Dynamic Range (SNR):** 123.5 dB @ 1ms Output
- **Total Harmonic Distortion (THD):** -118 dB over 2 KHz Sampling Bandwidth
- **Power Performance:**
  - Single-S Chipset: 70 mW per acquisition channel
  - Total-S Chipset: 60 mW per acquisition channel

A property of these chipsets is the THD performance variance as the gain setting is increased in the programmable gain amplifier (PGA). This variance is attributed to the charge-kickback effect from the Δ-Σ modulator during switched-capacitor sampling of its analog inputs [1]. An artifact of the design, the charge-kickback from the Δ-Σ modulator affects the common-mode PGA loop gain, which in turn, affects the amplifier's distortion performance. This charge-kick effect, however, can be reduced with the addition of common-mode capacitors. Using a standard CDB5378 evaluation board, the following Single-S THD performance over the complete CS3301/02 PGA gain setting range was measured:

PGA Gain Setting	Single-S THD Performance
1x.	-125.21 dB
2x.	-118.16 dB
4x.	-112.02 dB
8x.	-109.43 dB
16x.	-108.69 dB
32x.	-107.42 dB
64x.	-105.31 dB

By modifying the CDB5378 evaluation board as demonstrated in this application note, a THD performance improvement ranging from 2-4 dB over the PGA gain setting can be realized.

3. CDB5378 SINGLE-S EVALUATION SYSTEM

The Single-S and Total-S chipset provides single-channel and multi-channel (up to 4 sensors per chipset) analog-to-digital data acquisition for high-resolution seismic and geophysical measurement systems. Single-S offers a programmable differential gain amplifier (PGA) specialized for land or marine applications, a fourth-order Δ-Σ modulator, and a multi-function digital filter with an integrated PLL. Combined with a dedicated test DAC for sensor gain and offset calibration, this chipset enables geophysical systems designers to quickly design complete end-to-end synchronous, highly-integrated and customized solutions. The Total-S chipset provides the same performance, but uses a four-channel digital filter to support up to four sets of PGAs and Δ-Σ modulators.

The Single-S acquisition channel is depicted in Figure 1. A differential sensor (typically a geophone or hydrophone sensor) is connected to the CS3301 amplifier. This analog signal is amplified by the PGA and fed into the Δ-Σ modulator, where the analog to digital (A/D) conversion occurs. After A/D conversion, the Δ-Σ modulator outputs a 1-bit oversampled data stream to the digital filter for decimation and filtering. The digital filter, in turn, transfers 24-bit digitally coded samples at a programmed output rate to the end user via system telemetry.

The CDB5378 customer demonstration board [6] provides full-feature evaluation of the Single-S chipset consisting of the CS3301 geophone amplifier, the CS5373A single-channel modulator + test DAC, and the CS5378 digital filter + PLL. It comes complete with an on-board microcontroller and PC evaluation software for ease of configuration, testing, and signal analysis. For marine applications that require the CS3302 hydrophone amplifier, the CDB5378 requires a simple drop-in replacement of the CS3301 with a single pin signal re-assignment.

4. CS5373A ANTI-ALIAS FILTER CIRCUIT

In the existing CDB5378 evaluation system, a simple first-order anti-alias filter is required at the front-end of the CS5373A modulator as shown in Figure 2. The anti-alias filter consists of the following RC network:

- R_{AA} = 680 Ω (internal to CS3301/02)
- C_{diff} = 20 nF differential-mode (DM) capacitance

The placement and routing of these components are critical for optimum performance. Quad-group routing of the RC filter components and use of high-linearity capacitors (e.g. C0G) are required. Failure to follow these two guidelines can result in a decrease of THD performance by 15 dB or greater.

The RC filter is mainly used for bandwidth-limiting the analog input signals to provide low THD and to prevent modulator instability. In addition to ensuring out-of-band signals are eliminated, however, the anti-alias filter capacitors help eliminate the CS5373A modulator 'charge-kick' that the CS3301 amplifier observes during switched capacitor sampling. This residual 'charge-kick', in turn, can affect the amplifier's common-mode performance. To provide greater isolation between the CS3301 amplifier and the CS5373A modulator, common-mode (CM) capacitors are added to the system as shown in Figure 3. For evaluation purposes, C_{CM} = 10nF.

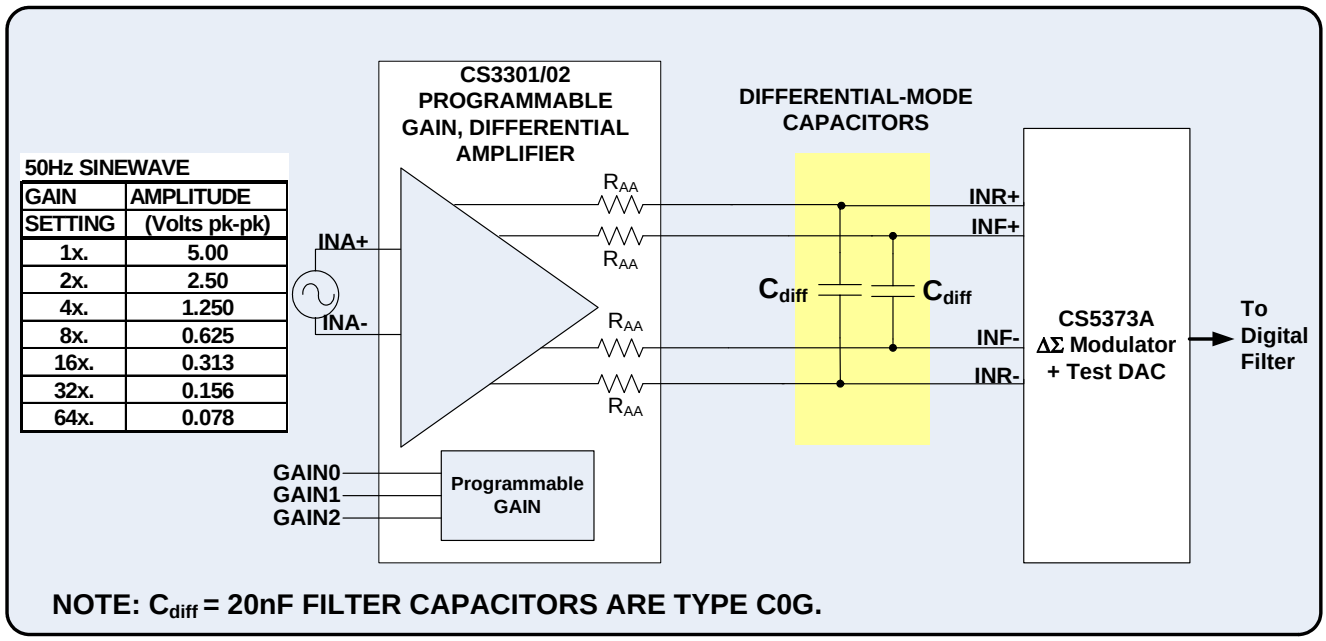

Figure 2. Existing CS5373A Modulator Anti-alias Filter Circuit

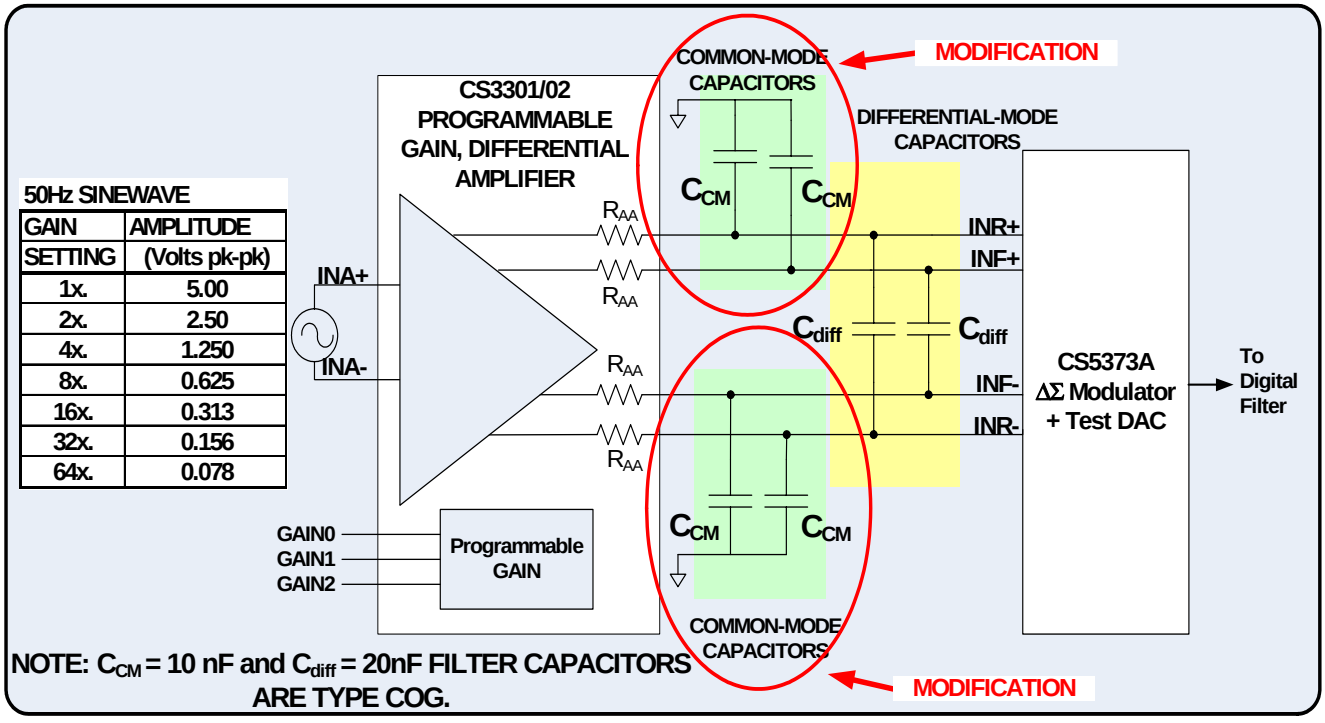

Figure 3. Modified CS5373A Modulator Anti-alias Filter Circuit

5. CDB5378 LAB SET-UP

CDB5378 includes simple-to-use PC Seismic GUI evaluation software. The Seismic GUI software was setup to evaluate system performance as shown in Figure 4. The Single-S chipset was configured with a 2 millisecond output sampling rate, and with binary-weighted gains of 1x to 64x applied on the CS3301/02 amplifier.

CDB5378 measurements were taken using five sample CS3301 amplifier parts. The test setup uses an external 50 Hz sine wave source with amplitude adjusted such that the CS5373A Δ-Σ modulator receives a full-scale input of 5.0 volts peak-to-peak (Vpp), regardless of the PGA gain setting. For each CS3301 PGA device, five data sets are acquired (4096 samples per data set), post-processed (using a 7-term Hodie window), and averaged.

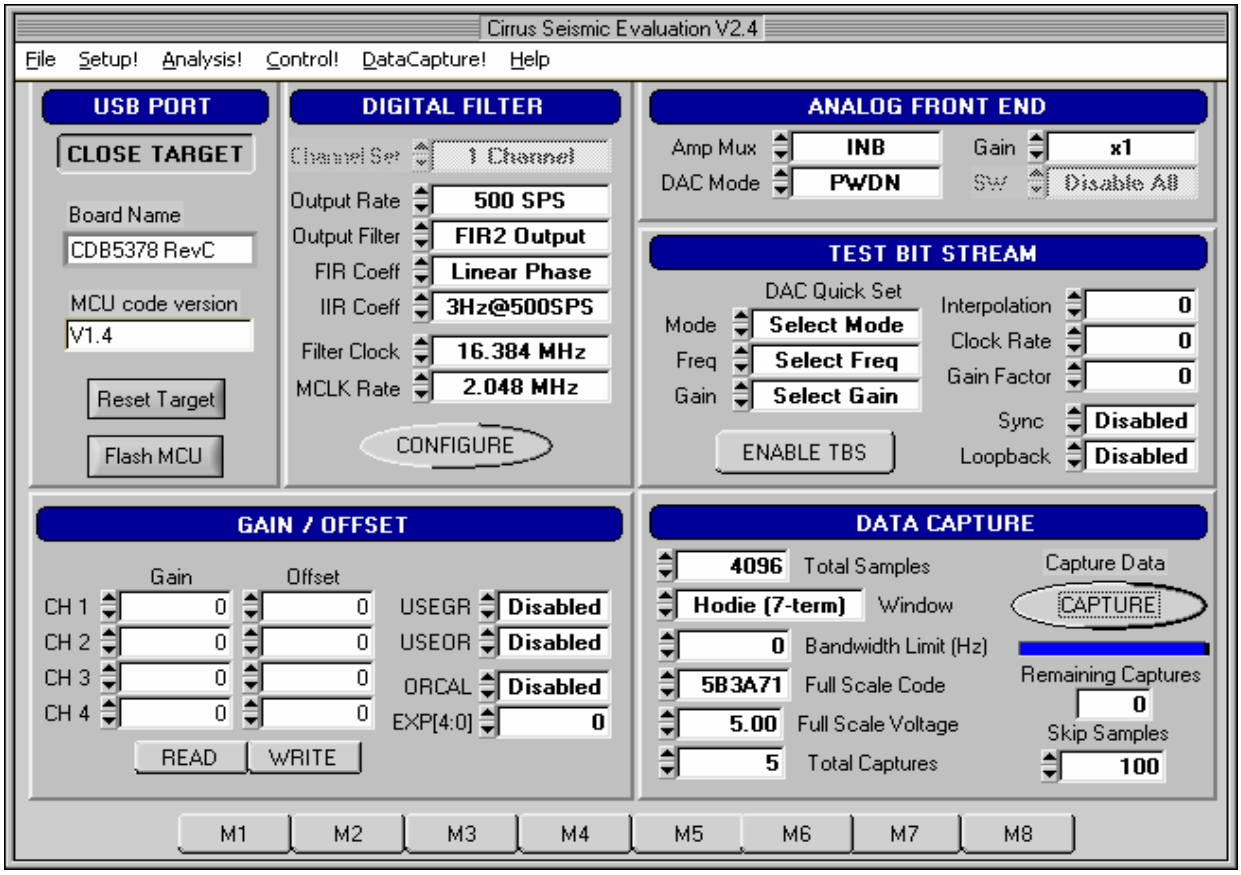

Figure 4. Seismic GUI Software Set-up for CDB5378 Measurements

6. CDB5378 LAB RESULTS

Results displayed in Figure 5 show an average THD performance improvement of +2 dB to +4 dB over the majority (4x to 64x) amplifier gain ranges when using CM and DM capacitors versus performance with DM capacitors only. For the 2x gain setting, there is a small loss of performance (roughly 2 dB to 3 dB); however, the CDB5378's mean THD performance measures -115dB, well above specification limits.

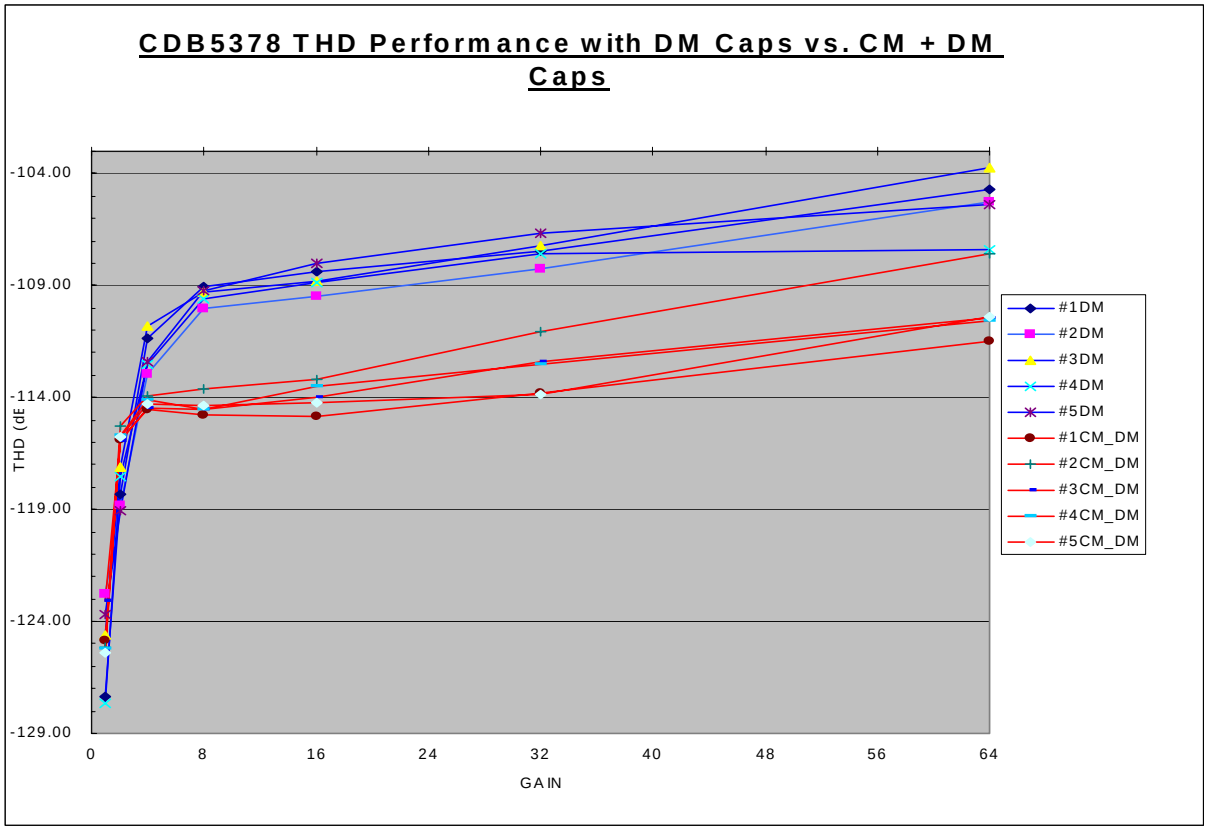

Figure 5. CDB5378 THD Performance with DM vs. DM+CM Anti-alias Capacitors

7. CONCLUSION

A property of the industry-leading Single-S and Total-S seismic chipsets is the THD performance variance with increased gain setting in the programmable gain amplifier (PGA).

This application note demonstrated how to increase the Single-S and Total-S exceptional THD performance over the possible PGA gain settings. Optimized performance is achieved by adding simple common-mode filter capacitors on the seismic chipset's Δ-Σ modulator analog inputs. Using a modified Single-S customer demonstration board (CDB5378) to obtain performance data, lab results indicate a THD boost of 2 dB (4x gain) to 4 dB (64x gain) is achievable. These results extend to the Total-S chipset because the CS5371/72 and the CS5373A share the same Δ-Σ modulator architecture.

8. REFERENCES

[1] Data sheet, *"CS5271/72 Low-power, High-performance Δ-Σ modulators"*
http://www.cirrus.com/en/products/pro/areas/PA78.html

[2] Data sheet, *"CS3301 Low-noise, Programmable Gain, Differential Amplifier"*
http://www.cirrus.com/en/products/pro/areas/PA78.html

[3] Data sheet, *"CS3302 High-Z, Programmable Gain, Differential Amplifier"*
http://www.cirrus.com/en/products/pro/areas/PA78.html

[4] Data sheet, *"CS4373A Low-power, High-performance Δ-Σ Test DAC"*
http://www.cirrus.com/en/products/pro/areas/PA78.html

[5] Data sheet, *"CS5376A Low-power, Multi-channel Decimation Filter"*
http://www.cirrus.com/en/products/pro/areas/PA78.html

[5] Data sheet, *"CS5378 Low-power, Single-channel Decimation Filter"*
http://www.cirrus.com/en/products/pro/areas/PA78.html

[6] Data sheet, *"CDB5378 Single-channel Seismic Evaluation System"*
http://www.cirrus.com/en/products/pro/areas/PA78.html

9. REVISION HISTORY

Release	Date	Changes
REV1	FEB 2007	Initial Release
REV2	JUN 2007	Update Cirrus Logic trademark acknowledgments.

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For all product questions and inquiries, contact a Cirrus Logic Sales Representative.
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